REMARKS

Reconsideration of the application as amended herein is respectfully requested. Claims 1-5 are pending.

Rejection under 35 U.S.C. § 132

The Office Action has objected to the Amendment filed on January 31, 2005 because it allegedly contains new matter. Applicant respectfully traverses this objection. The text objected to is a quote from U.S. Patent No. 5,551,013. See Column 10, lines 55-62. U.S. Patent 5,551,013 is incorporated by reference into the present application. This incorporation by reference was made at the time the present application was filed. Thus, any disclosure present in U.S. Patent No. 5,551,013 is part of the disclosure of the present application and importing text from that patent into the present application does not constitute the addition of new matter.

Thus, Applicant respectfully submits that the January 31, 2005 amendment did not add new matter and requests that this objection be withdrawn.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action has rejected claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over Catlin in view of Nishikdawa. Applicant respectfully traverses this rejection. In order for a combination of references to render a claim obvious, they must be properly combinable and must teach or suggest each and every limitation of the claim. Even if Catlin and Nishikdawa are properly combinable (which Application respectfully submits is not the case) they fail to teach limitations required by each of the claims.

Catlin is directed to a microprocessor emulator. Applicant notes that one having ordinary skill in the art would recognize that a microprocessor emulator does not execute programs that correspond to a logic design, as is required by each of the claims. In fact, Catlin makes clear that its purpose to allow software development in a processor-based product such as a PC. Catlin teaches that a microprocessor is disposed on a printed circuit board that has a cable that extends from that board to a PC motherboard or the like which facilitates software development:

> Software development for the microcomputer is sometimes carried out using an in-circuit emulator (the emulator). The emulator is a separate computer system having an interface with terminals that correspond to the processor pins. A multi-conductor cable is connected to the interface terminals at one end and terminates in a plug which is inserted into the processor socket. The emulator plug's pins correspond to the processor's pins. The emulator computer emulates the processor and effectively substitutes itself for the processor (which was removed from its socket or was never inserted into it). The emulator computer has various capabilities beyond that of the processor, and thus provides the software developer with a broad range of diagnostic features.

Catlin, Col. 1, lines 25-39. Catlin says nothing about executing emulation programs *corresponding to a logic design*, which is required by each of the claims. Moreover, each claim of the present application is directed to determining cable length between printed circuit boards of the emulation system itself. For example, claim 1 requires that the "at least two printed circuit boards" of the hardware logic emulation system be "interconnected by a multi-conductor cable". Similarly, claim 5 requires that the emulation system itself have "a first printed circuit board … electrically communicating with a second printed circuit board … via the multi-conductor cable". In contrast, the cable in Catlin extends from the emulator itself (reference numeral 50 in Catlin) to some other printed circuit board (reference numeral 40 in Catlin), which is not part of the emulator:

> FIG. 2 is block diagram illustrating in-circuit emulation of processor 20 with processor 20 mounted to a circuit board 40. The processor is shown as having pins 12a-b and isolation pin 25 as shown in FIG. 1B. As noted above, this is a simplified view. Pins 12a-12d are shown as connected to respective off-chip blocks 42a-d which may be passive circuit elements, active circuit elements, or connectors.
>
> An in-circuit emulator 50 (referred to as the emulator) includes an emulator computer 52 coupled to an emulator interface 55. Emulator interface 55 has a set of emulator terminals 57a-d that correspond to pins 12a-d on processor 20. Emulator computer 52 receives signals that are communicated to the input terminals on the emulator interface and generates signals that are driven on the output terminals of the emulator interface according to the same protocol that characterizes processor 20. A cable 60 contains conductors 62a-d coupled at respective first ends to emulator terminals 57a-d. The cable terminates in a set of contacts 65a-d coupled to respective second ends of conductors 62a-d. The contacts are mounted and configured so that the contact for a given conductor engages the processor pin corresponding to the emulator interface terminal for that conductor.

Catlin, Col. 3, lines 34-58.

The Office Action points to Col. 1, lines 15-24 from Catlin as allegedly teaching a multiple board emulation system:

> Reduced to essentials, however, the processor can be viewed as a device that provides defined output signals on various of its pins in response to input signals on various of its pins according to a particular (albeit complex) protocol. A device is said to emulate the processor if it has a set of pins or terminals corresponding to those of the processor and provides output signals on its terminals in response to input signals on its terminals according to the same protocol as the processor.

Applicant respectfully submits that this citation says absolutely nothing about an emulator comprised of multiple boards.

In addition, contrary to what is alleged in the Office Action, Catlin says nothing about interchanging the inputs or outputs of at least one pair of conductors, as is required by all the claims. The Office Action states that this passage from Catlin supplies such a teaching:

> Bidirectional pin 12a has an associated input buffer 15a and an associated output buffer 17a. Output pins 12b and 12c have respective associated output buffers 17b and 17c. Input pin 12d has an associated input buffer 15d.

Catlin, Col. 2, lines 43-48. Applicant respectfully submits that neither this passage nor any other in Catlin say anything about interchanging the inputs or outputs of at least one pair of conductors. In fact, all this quote states is that the pins have input and output buffers, which Applicant respectfully submits says absolutely nothing about interchanging the inputs or outputs of conductor pairs.

In addition, Catlin says nothing about compiling emulation programs to account for the interchanged conductors. First, as discussed, Catlin says nothing about interchanging conductors, meaning that Catlin need not account for them. Secondly, as also discussed, the "emulation programs" of a hardware logic emulation system are fundamentally different than the types of programms a microprocessor emulator would be running. Finally, the quote in the Office Action that allegedly supplies a teaching for accounting for the interchanged conductors in fact makes no such teaching:

> FIG. 1C is a fragmentary circuit schematic of an alternative embodiment for the isolation circuitry. In this embodiment, the processor is not provided with a single dedicated ISOLATE pin, but rather is provided with a number of test pins used for various test purposes, wherein the combination of input values specifies the particular operation. In the specific embodiment shown, a pair of test pins 35a and 35b receive test signals TEST1* and TEST2*. The test signals communicate via input buffers 36a and 36b to decoding circuitry, a portion of which is shown. Specifically, a gate 37 drives node 27 low when TEST1* and TEST2* are both

> active (low), which disables the output buffers as in the embodiment of FIG. 1B.

Catlin, Col., 3, lines 19-33. All this quote teaches is that test pins receive signals. It says absolutely nothing about accounting for interchanged conductors.

Finally, as even the Office Action notes, Catlin says absolutely nothing about determining cable length and as seen above, fails to teach or suggest any of the steps required by the claims. Indeed, Applicant respectfully submits that the fact that Catlin says nothing about determining cable length means that a person having ordinary skill in the art would never refer to Catlin when attempting to develop a system that in fact determines cable length.

Applicant also respectfully submits that Nishikdawa has nothing to do with determining thelengths of cables used to interconnect printed circuit boards. First of all, Nishikdawa is directed to *reducing wire length of metal interconnect lines fabricated onto on integrated circuit*:

> In designing a semiconductor integrated circuit represented by an IC, constituent elements (to be referred to as "objects" herein) such as semiconductor objects and wires are laid out in a limited area. To make a compact semiconductor integrated circuit and reduce the manufacturing cost in such design, it is important to minimize the layout area.

Nishikdawa, Col. 1, lines 14-21. Applicant respectfully submits that metal wires fabricated onto semiconductor chips are completely different than cables used to interconnected printed circuit boards. Thus, Nishikdawa is not properly combinable with Catlin. Moreover, the fact Nishikdawa is directed to metal lines fabricated onto semiconductor devices means that it does not teach or suggest anything relating to cables used to interconnect printed circuit boards. They are completely different structures.

In addition, Nishikdawa does not teach or suggest anything remotely similar to determining cable length. First, since Nishikdawa says nothing about cables, it cannot possibly

teach anything about determining their length. Moreover, the quote provided by the Office Action (Nishikdawa, Col. 6, lines 1-35) as allegedly supplying a teaching for determining cable length, in facts says nothing of the kind. All this quote says is that wire lengths on a semiconductor chip can be reduced if circuit blocks are placed intelligently:

> The present invention has been made in consideration of the above situation, and has as its object to efficiently specify objects to be moved for cost reduction of wires in a wire length minimization apparatus and method of performing wire length minimization which is performed next to area minimization processing in one-dimensional compaction processing for the layout of a semiconductor integrated circuit.
>
> It is another object of the present invention to effectively minimize the wire length by using a variety of combinations of vertexes to be moved for wire length minimization in a constraint graph, as compared to the prior art.
>
> It is still another object of the present invention to provide a wire length minimization technique with good convergence properties.
>
> It is still another object of the present invention to effectively minimize the total wire length while avoiding an excess change in layout.
>
> According to the present invention, there is provided a wire length minimization method of moving an object and a wire in a wiring pattern formed by connecting objects with wires, in accordance with a load representing a performance of wire length minimization considering a priority of each wire, thereby minimizing a wire length, the method comprising the following steps of:
>
> forming a tree having, as nodes, a plurality of objects having a predetermined positional relationship;
>
> calculating, sequentially from a leaf side of the tree, a load of a parent node based on a load of a child node; and
>
> specifying objects and wires corresponding to a tree portion having a root node with a load satisfying a predetermined condition, and moving the specified objects and wires as a whole.

As is seen from the above, both Catlin and Nishikdawa are missing limitations present in all the claims of this application. Thus, even if Catlin and Nishikdawa are properly combinable (which as discussed, they are not), the combination fails to teach several limitations of the claims. Because limitations are missing, the combination of Catlin and Nishikdawa cannot render claims 1-5 obvious.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that the present application is in condition for allowance, which is respectfully requested. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (650) 614-7400. If additional fees are needed, the Office is authorized to charge Deposit Account No. 15-0665.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: August 3, 2005

By: Sanjeet Dutta
Sanjeet K. Dutta
Reg. No. 46,145

Four Park Plaza, Suite 1600
Irvine, California 92614-2558
(650) 614-7660